

# Am26123•Am54/74123

## Dual Retriggerable Resettable Monostable Multivibrator

### Key Characteristics

Retriggerable 0 to 100% duty cycle.  
Ons to  $\infty$  output pulse width range.

Am26123 guaranteed pulse width change of less than 1% over 0°C to +70°C temperature range.

- Am26123 outputs immune to noise triggering the monostable at the RC timing nodes.
- 100% reliability assurance testing in compliance with MIL-STD-883.

### FUNCTIONAL DESCRIPTION

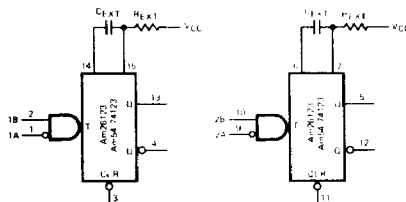
The Am26123 and the Am54/74123 are dual retriggerable resettable monostable multivibrators. The output pulse-width duration and accuracy are determined by external timing components. The Am26123 is pin compatible with the Am54/74123 but features two major improvements:

Pulse width stability of  $\pm 1\%$  or better is guaranteed over 0°C to +70°C for the Am26123.

The Am26123 incorporates an output latch which offers immunity to spurious output changes in the quiescent state due to coupling of external noise at the timing capacitor nodes.

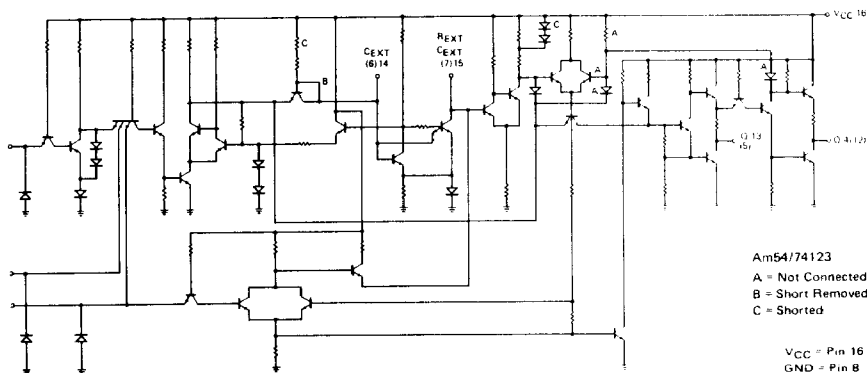
An active-LOW A input and an active-HIGH B input are electrically coupled in an AND gate on the trigger input of each device. A LOW on the clear input resets the monostable to the normal LOW quiescent state regardless of the A and B inputs.

### LOGIC DIAGRAM



VCC = Pin 16  
GND = Pin 8

### Am26123 SCHEMATIC DIAGRAM



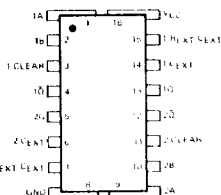
Am54/74123  
A = Not Connected  
B = Short Removed  
C = Shorted

VCC = Pin 16  
GND = Pin 8

### ORDERING INFORMATION

Package Type	Temperature Range	Am26123 Order Number	Am54/74123 Order Number
Standard DIP	0°C to +70°C	AM26123PC	SN74123N
Plastic DIP	0°C to +70°C	AM26123DC	SN74123J
Dice	0°C to +70°C	AM26123XC	SN74123X
Plastic DIP	-55°C to +125°C	AM26123DM	SN54123J
Plastic Flat Pack	-55°C to +125°C	AM26123FM	SN54123W
Dice	-55°C to +125°C	AM26123XM	SN54123X

### CONNECTION DIAGRAM Top View



**MAXIMUM R**
**3S** (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	-0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	-0.5 V to +V <sub>CC</sub> max
DC Input Voltage	-0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	-30 mA to +5.0 mA

**ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (Unless Otherwise Noted)

 Am26123XC, Am74123  
 Am26123XM, Am54123

 T<sub>A</sub> = 0°C to +70°C

 T<sub>A</sub> = -55°C to +125°C

 V<sub>CC</sub> = 5.0 V ± 5% (COM'L)

 V<sub>CC</sub> = 5.0 V ± 10% (MIL)

MIN. = 4.75 V

MIN. = 4.5 V

MAX. = 5.25 V

MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage					V
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = MIN., I <sub>I</sub> = -12 mA			0.8	V
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = MIN., I <sub>OH</sub> = -800 μA (Note 5)	2.4	4.0	-1.5	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN., I <sub>OL</sub> = 16 mA (Note 5)		0.22	0.4	V
I <sub>I</sub>	Input Current at Maximum Input Voltage	V <sub>CC</sub> = MAX., V <sub>I</sub> = 5.5 V			1.0	mA
I <sub>IH</sub> (Note 3)	Input HIGH Current	A or B	V <sub>CC</sub> = MAX., V <sub>I</sub> = 2.4 V	5	40	μA
		Clear		10	80	
I <sub>IL</sub> (Note 3)	Input LOW Current	A or B	V <sub>CC</sub> = MAX., V <sub>I</sub> = 0.4 V	-1.0	-1.6	mA
		Clear		-2.0	-3.2	
I <sub>OS</sub>	Output Short Circuit Current (Note 4)	V <sub>CC</sub> = MAX. (Note 5)	Am54/74123 V <sub>OUT</sub> = 0.0 V	-10	-40	mA
			Am26123 V <sub>OUT</sub> = 1.0 V, T <sub>A</sub> = 25°C			
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = MAX. (Notes 6 & 7)	46	66	mA	

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.  
 2. Typical limits are V<sub>CC</sub> = 5.0 V, 25°C ambient and maximum loading.  
 3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).  
 4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 5. Ground C<sub>ext</sub> to measure V<sub>OH</sub> at Q, V<sub>OL</sub> at  $\bar{Q}$ , 0 V I<sub>OS</sub> at Q. C<sub>ext</sub> is open to measure V<sub>OH</sub> at  $\bar{Q}$ , V<sub>OL</sub> at Q, 0 V I<sub>OS</sub> at  $\bar{Q}$ . (On the Am26123, the input must be triggered also.)  
 6. I<sub>CC</sub> is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C<sub>ext</sub> = 0.02 μF and R<sub>ext</sub> = 25 kΩ.  
 7. Quiescent I<sub>CC</sub> is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C<sub>ext</sub> = 0.02 μF, and R<sub>ext</sub> = 25 kΩ.

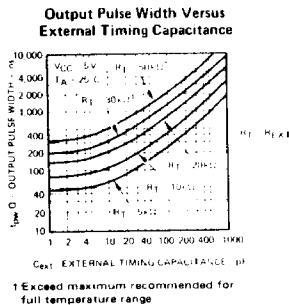
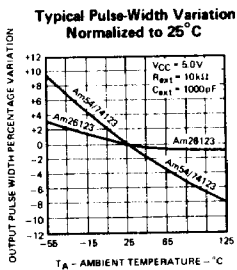
**Switching Characteristics** (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units	
t <sub>PLH</sub>	A to Q	C <sub>ext</sub> = 0, R <sub>ext</sub> = 5 kΩ C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω		22	33	ns	
t <sub>PHL</sub>	A to $\bar{Q}$			30	40	ns	
t <sub>PLH</sub>	B to Q			19	28	ns	
t <sub>PHL</sub>	B to $\bar{Q}$			27	36	ns	
t <sub>PLH</sub>	Clear to Q			30	40	ns	
t <sub>PHL</sub>	Clear to $\bar{Q}$			18	27	ns	
t <sub>pwQ</sub> (MIN.)	Minimum Pulse Width Q Output				45	65	ns
t <sub>pw</sub>	A or B inputs HIGH			40		ns	
t <sub>pw</sub>	A or B inputs LOW			40		ns	
t <sub>pw</sub>	Clear LOW			40		ns	
t <sub>pwQ</sub>	Pulse Width Q Output		C <sub>ext</sub> = 1000 pF, R <sub>ext</sub> = 10 kΩ C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω	3.08	3.42	3.76	μs

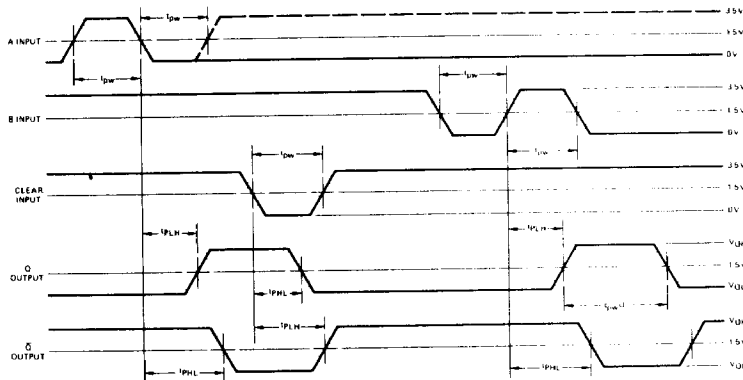
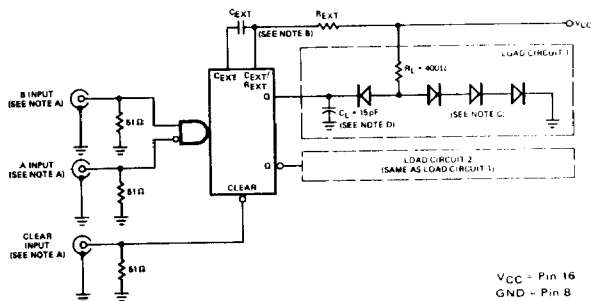
**Am26123 Only**

4-88	Δt <sub>pw</sub> (T)	Maximum Change of t <sub>pwQ</sub> Over Temperature Range 0°C to +70°C	C <sub>ext</sub> = 1000 pF, R <sub>ext</sub> = 10 kΩ C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω		±0.5	±1.0	%
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 N  
A  
B  
C  
D



### SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



**Notes:**  
 The pulse generators have the following characteristics:  $t_r \leq 10ns$  (10% to 90% level),  $t_f \leq 10ns$ ,  $PRR \leq 1MHz$ , duty cycle  $\leq 50\%$ ,  $Z_{OUT} \approx 50\Omega$ .  
 See Test Conditions, switching characteristics table, for values of  $R_{EXT}$  and  $C_{EXT}$ .  
 All diodes are 1N3064.  
 $C_L$  includes probe and jig capacitance.

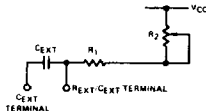
## OPERATING CONDITIONS

### TIMING

1. Timing components  $C_{EXT}$  and  $R_{EXT}$  values.

Operating Temperature Range		
	0°C to 70°C	-55°C to +125°C
$R_{EXT}$ MIN.	5kΩ	5kΩ
$R_{EXT}$ MAX.	50kΩ	25kΩ
$C_{EXT}$	any value	any value

2. Remote adjustment of timing.



$$\begin{aligned} R_1 + R_2 &= R_{EXT} \\ R_1 &\geq R_{EXT} \text{ MIN.} \\ R_2 &< R_{EXT} \text{ MAX.} - R_1 \end{aligned}$$

In the above arrangement,  $R_1$  and  $C_{EXT}$  should be as close as possible to the device pins to minimize stray capacitance and external noise pickup. The variable resistor  $R_2$  can be located remotely from the device if reasonable care is used.

3. Pulse width change measurements.

The pulse width  $t_{PWQ}$  is specified and measured with components of better than 0.1% accuracy. If measurements are made with reduced component tolerances, the expected accuracy should be adjusted accordingly.

4. Timing for  $C_{EXT} < 1000$  pF.

When using capacitor of less than or equal to 1000 pF in value, the output pulse width should be determined from the output pulse width versus external timing capacitance graph.

5. Timing for  $C_{EXT} > 1000$  pF.

For capacitors of greater than 1000 pF in value, the output pulse width,  $t_{PWQ}$ , is determined by

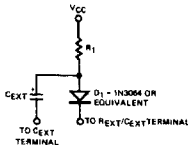
$$t_{PWQ} = 0.32 R_{EXT} C_{EXT} \left(1 + \frac{0.7}{R_{EXT}}\right)$$

where

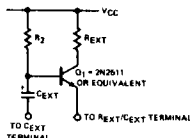
$$\begin{aligned} R_{EXT} &\text{ is in kilohms} \\ C_{EXT} &\text{ is in picofarads} \\ t_{PWQ} &\text{ is in nanoseconds} \end{aligned}$$

6. Protection of electrolytic timing capacitors.

If the electrolytic capacitor to be used as  $C_{EXT}$  cannot withstand 1.0 volt reverse bias, one of the following two circuit techniques should be used to protect the electrolytic capacitor from the reverse voltage.



$$4-90 \quad R_1 < 0.6 \times R_{EXT} \text{ MAX.}$$



$$R_2 < 0.7 \times h_{FEQ1} \times R_{EXT}$$

The output pulse width,  $t_{PWQ}$ , for the diode circuit modifies the previous timing equation as follows:

$$t_{PWQ} = 0.28 R_1 C_{EXT} \left(1 + \frac{0.7}{R_1}\right)$$

The output pulse width for the transistor circuit is

$$t_{PWQ} = 0.30 \times R_2 \times C_{EXT} \left(1 + \frac{0.7}{R_2}\right)$$

Notice that the transistor circuit allows values of timing resistor  $R_2$  larger than the  $R_{EXT} \text{ MIN} < R_{EXT} < R_{EXT} \text{ MAX.}$  to obtain longer output pulse widths for a given  $C_{EXT}$ .

## TRIGGER AND RETRIGGER

1. Triggering.

The minimum pulse width signal into input A or input B to cause the device to trigger is 40ns. Refer to the truth table for the appropriate input conditions.

2. Retriggering.

The retriggered pulse width,  $t_{PWRQ}$ , is the time during which the output is active after the device is retriggered during a timing cycle. It differs from the initial pulse width  $t_{PWQ}$  timing equation as follows.

$$t_{PWRQ} = t_{PWQ} + t_{PLH}$$

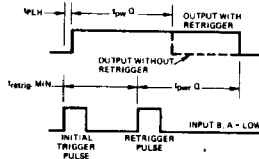
where  $t_{PLH}$  is the propagation delay time from the A or B input to the output.

For values of  $t_{PWQ}$  greater than about 500ns,  $t_{PLH}$  can be ignored.

3. Rapid retriggering.

A minimum retriggering time does exist. That is, the device cannot be retriggered until a minimum recovery time has elapsed. The minimum retrigger time is defined by

$$\begin{aligned} t_{retrig} \text{ MIN.} &= 0.224 C_{EXT} \\ C &\text{ is in picofarads} \\ t &\text{ is in nanoseconds} \end{aligned}$$



4. Output Latch.

The Am26123 incorporates an output latch that can be triggered only by the input trigger gate via the A or B inputs. Thus, spurious output pulses caused by external noise on the  $C_{EXT}$  nodes are eliminated during the quiescent state. This feature is extremely valuable in many high noise environment systems.

## CLEAR

A LOW on the clear inputs terminates the timing cycle. It also resets the output latch on the Am26123. A new trigger cycle cannot be initiated while the clear is LOW. With the clear HIGH, the device is under the command of the A and B inputs.

**TRUTH TABLE**  
Am26123 • Am54/74123  
For Each Monostable

Clear	A	B	Q	$\bar{Q}$
L	X	X	L	H
H	H	X	L	H
H	L	↑		
H	X	L	L	H
H	↓	H		

H = HIGH    X = Don't Care  
L = LOW  
↑ = LOW-to-HIGH transition  
↓ = HIGH-to-LOW transition  
 = LOW-HIGH-LOW pulse  
 = HIGH-LOW-HIGH pulse

**MSI INTERFACING RULES**

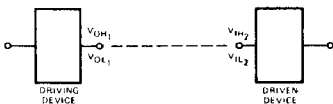
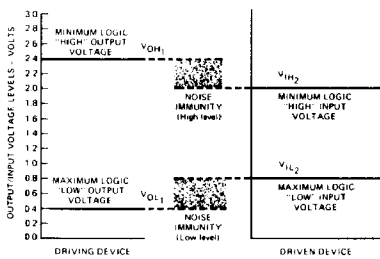
Interfacing Digital Family	Equivalent Input Unit Load	
	HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

**Am26123 • Am54/74123 LOADING RULES**

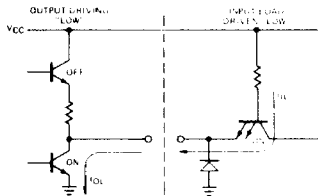
Input/Output	Pin No.'s	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
1A	1	1	-	-
1B	2	1	-	-
1 CLEAR	3	2	-	-
1 $\bar{Q}$	4	-	20	10
2Q	5	-	20	10
2 C <sub>ext</sub>	6	-	-	-
2 R <sub>ext</sub> /C <sub>ext</sub>	7	-	-	-
GND	8	-	-	-
2A	9	1	-	-
2B	10	1	-	-
2 CLEAR	11	2	-	-
2 $\bar{Q}$	12	-	20	10
1Q	13	-	20	10
1 C <sub>ext</sub>	14	-	-	-
1 R <sub>ext</sub> /C <sub>ext</sub>	15	-	-	-
VCC	16	-	-	-

**INPUT/OUTPUT INTERFACE CONDITIONS**

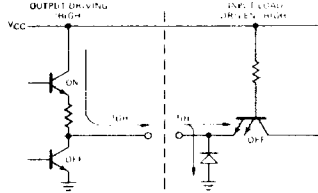
**Voltage Interface Conditions – LOW & HIGH**



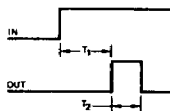
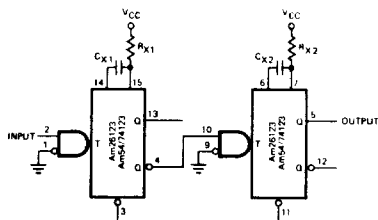
**Current Interface Conditions – LOW**



**Current Interface Conditions – HIGH**

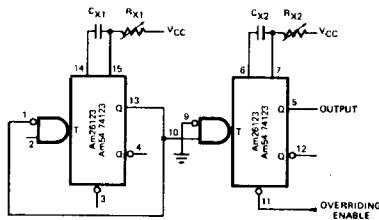


## APPLICATIONS



### Delayed Pulse Generation

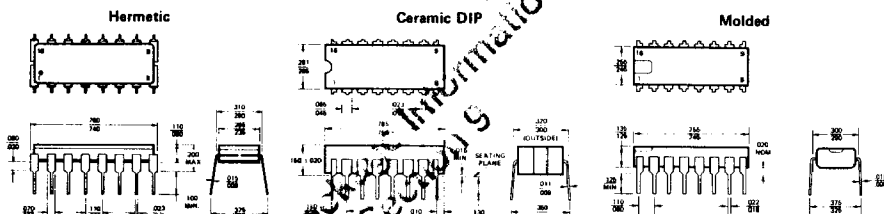
The first monostable determines the time  $T_1$  before the initiation of the output pulse. The second monostable determines  $T_2$ , the output pulse width.



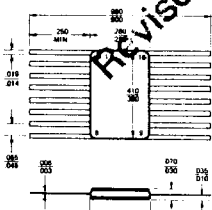
### Pulse Generator

The output frequency produced with the above configuration is determined by  $C_{X1}$  and  $R_{X1}$ , while the pulse width is determined by  $C_{X2}$  and  $R_{X2}$ . Monostable 1 forms an astable multivibrator with an output pulse width of approximately 25 ns, while monostable 2 extends the pulse width to the required value.

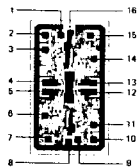
## PHYSICAL DIMENSIONS



### Flat Package



### Metallization and Pad Layout



DIE SIZE 0.050" X 0.088"



**ADVANCED  
MICRO  
DEVICES INC.**  
901 Thompson Place  
Sunnyvale  
California 94086  
(408) 732-2400  
TWX: 910-339-9280  
TELEX: 34-8308

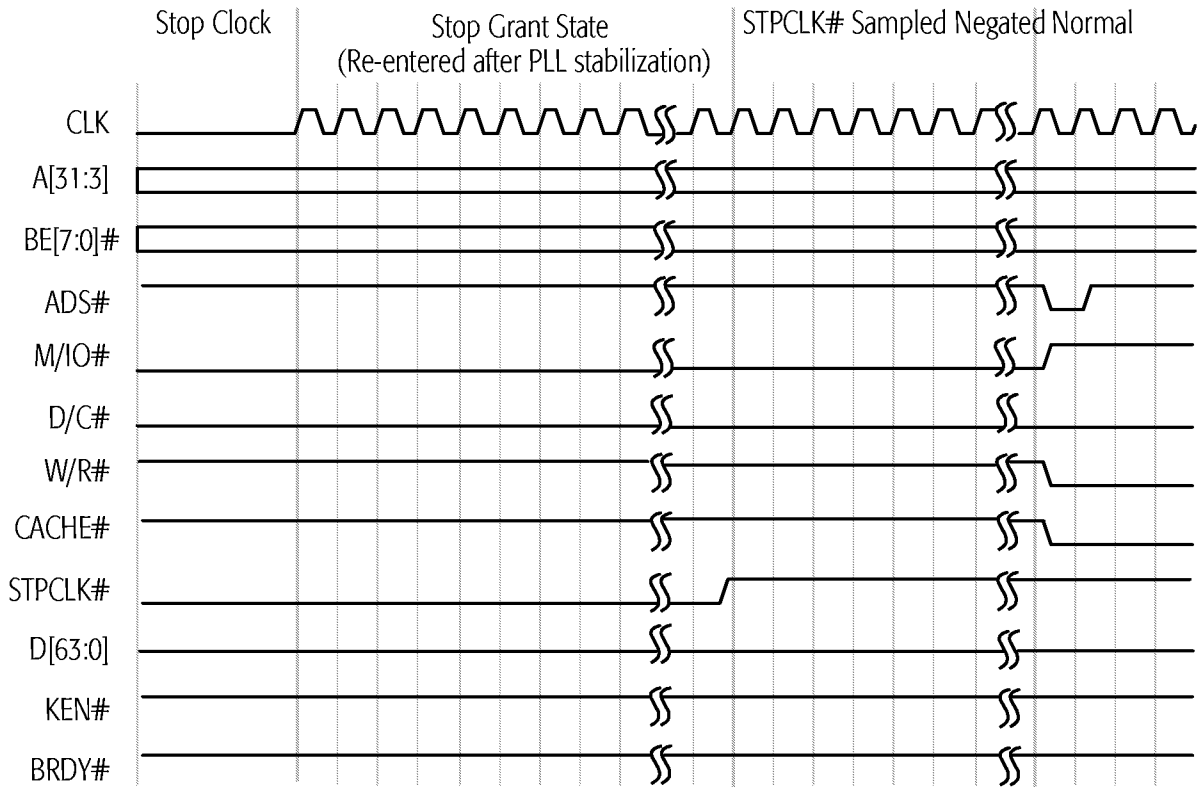


Figure 75. Stop Grant and Stop Clock Modes, Part 2

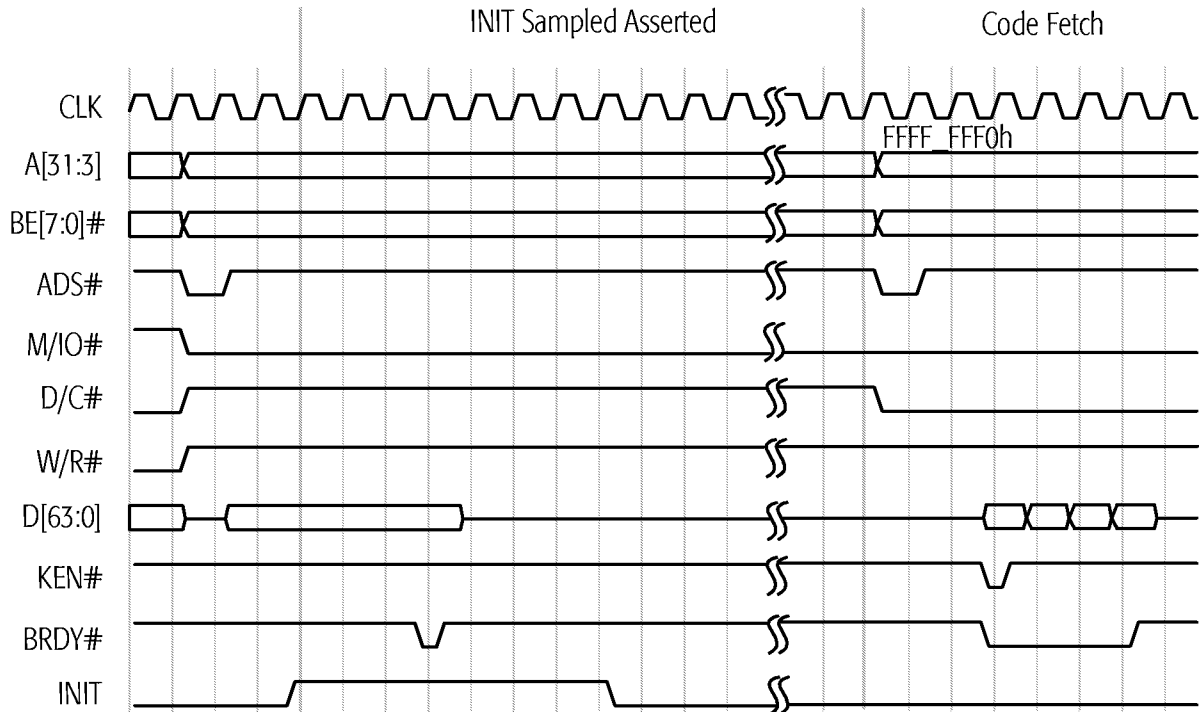
**INIT-Initiated  
Transition from  
Protected Mode to  
Real Mode**

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF\_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF\_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.





**Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode**



## 6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF\_FFF0h to start instruction execution.

### 6.1 Signals Sampled During the Falling Transition of RESET

- FLUSH#** FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF\_FFF0h to start instruction execution. (See “Built-In Self-Test (BIST)” on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See “Tri-State Test Mode” on page 218 and “FLUSH# (Cache Flush)” on page 103 for more details.)
- BF[2:0]** The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See “BF[2:0] (Bus Frequency)” on page 92 for the processor-clock to bus-clock ratios.)
- BRDYC#** BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See “BRDYC# (Burst Ready Copy)” on page 95 for more details.)

## 6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V<sub>CC</sub> reach specification. (See “CLK Switching Characteristics” on page 255 for clock specifications. See “Electrical Data” on page 247 for V<sub>CC</sub> specifications.)

During a warm reset while CLK and V<sub>CC</sub> are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

## 6.3 State of Processor After RESET

### Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

**Table 31. Output Signal State After RESET**

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACK#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	—	—

### Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.